AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0027] with the following amended paragraph:

[0027] FIG. 2 shows a negative charge pump circuit 200 in accordance with another embodiment of the present invention. Pump circuit 200 includes a plurality of charge pump circuits 100(1)-100(n) of FIG. 1 that can be selectively connected in parallel to provide various levels of drive current to VNN. Each of the charge pump circuits 100(1)-100(n) includes inputs to receive OSC, ENA, ENB, and MODE, and can be used to generate various negative output voltages as described above with respect to FIG. 1. The output of each charge pump circuit 100 is connected to an input of a corresponding switching circuit 202, which in turn includes an output connected to VNN and a control terminal to receive a corresponding select signal SEL. Switching circuits ~~200(1)-200(n)~~ 202(1)-202(n) can be any suitable switching circuit or device. For some embodiments, switching circuits 202(1)-202(n) can be MOS transistors having gates responsive to SEL(1)-SEL(n), respectively. For one embodiment, switching circuits 202(1)-202(n) are PMOS transistors.

Please replace paragraph [0031] with the following amended paragraph:

[0031] For other embodiments of charge pump circuit 200, switching circuits 202 can be eliminated, and the select signals SEL_1 to SEL_n can be used to selectively enable or disable corresponding charge pump circuits 100(1)-100(n). For example, FIG. 3A shows one embodiment in which ENA can be gated with SEL in an AND gate 301 and ENB can be gated with SEL in an AND gate 302 to selectively disable the first and second charge pumps 110 and 120, respectively, in a corresponding charge pump circuit 100. FIG. 3B shows another embodiment in which each select signal SEL can be combined with ENA and OSC in a first AND gate 351 to generate OSC_A for a corresponding charge pump 100, and combined with ENB and OSC in a second AND gate ~~351~~ 352 to generate OSC_B for the corresponding charge

pump 100. For the exemplary embodiments of FIGS. 3A and 3B, asserting SEL (e.g., to logic high) enables the first and second charge pumps 110 and 120 of a corresponding charge pump circuit 100 by allowing OSC to pass thereto, while de-asserting SEL (e.g., to logic low) disables the first and second charge pumps 110 and 120 of the corresponding charge pump circuit 100 by forcing OSC to ground potential.